EGC-220 HW #4 Dr. Izadi

First Name: _____ Last Name: _____

15 PT.
Problem 1
Design a circuit that counts the number of 0's present in 4 inputs A, B, C and D. Its output is a multi-bit, representing that count in binary. For example, 0101 has two zeros and therefore the output should be a binary representing 2.

a. Write the truth table for this circuit.
b. Find the minimized logic equations in SOP and POS for each output
c. Draw the corresponding all NAND and all NOR gates logic diagram for this circuit. Label all inputs and outputs.

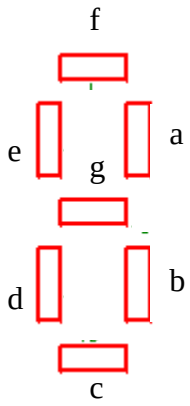
15 PT.
Problem 2
Design a circuit with inputs A,B,C, and D. Let the two inputs AB represent a two-bit number with A as the high order bit, and CD represent another two-bit number. That is, the values on AB represent four values 00 (0), 01 (1), 10 (2), and 11 (3). The circuit has three outputs: G, E, and L. Output G, E, and L should be 1 only if the number represented by AB is greater, equal, and less than the number represented by CD, respectively.

a. Write the truth table for this circuit.
b. Find the minimized logic equations in SOP and POS for each output
c. Draw the corresponding all NAND and all NOR gates logic diagram for this circuit. Label all inputs and outputs.

20 PT.
Problem 3
Design a circuit that can convert a 4-input BCD code into a Gray code.

a. Write the truth table for this circuit.
b. Find the minimized logic equations in SOP and POS for each output
c. Draw the corresponding all NAND and all NOR gates logic diagram for this circuit. Label all inputs and outputs.

25 PT.
Problem 4
There is an integrated circuit called a BCD-seven segment decode that takes 4 inputs and has seven output. The inputs represent a number between 0 and 9, and each of the seven outputs corresponds to one of seven LED's in a seven-segment display. A typical seven-segment display is shown below.



a. Write the truth table for each segment "a, b, c, d, e, f, g" with inputs A, B, C, and D. Make sure to adhere to the indicated segment notations.
b. Simplify each output in Minimum S.O.P.
c. Implement each output using all NAND gates.

15 PT.
Problem 5
Design a 1 out of 4 decoder with active low outputs and two enable lines, one active low and one active high.

15 PT.
Problem 6
Using the decoder in Problem 5, design a 1 out of 16 decoder with active low outputs.

15 PT.
Problem 7
Implement the following Boolean expression using a decoder and an OR gate – You may choose a decoder with active high or active low outputs.

$F(A, B, C, D) = \sum m\,(0, 1, 2, 4, 5) + d(3, 6)$

15 PT.
Problem 8
Implement the following Boolean expression using a decoder and a NAND gate.

$F(X, Y, Z, W) = \prod M(0, 6, 8, 13, 14) + d(2, 4, 10)$

15 PT.
Problem 9
Obtain the truth table for a 16 × 4 priority encoder with inputs $D_0 - D_{15}$, and output X, Y, Z, W, V (valid). Assume higher index has higher priority.

15 PT.
Problem 10
Design an 8 × 1 Mux.

15 PT.
Problem 11
Implement an 8 × 1 Mux using 2 × 1 Mux's.

15 PT.
Problem 12
Implement the following Boolean expression using an 8 × 1 Mux.

$F(A, B, C, D) = \sum m(4, 6, 7, 8, 12, 15)$

15 PT.
Problem 13
Repeat Problem 12 using a 4 × 1 Mux and external gates.

15 PT.
Problem 14
Implement the following functions using a PLE.

$F_1 = \sum m\ (0,2,5,7,8,10,12,13)$

$F_2 = \sum m\ (0,2,4,5,6,7,8,10,13,15)$

$F_3 = \sum m\ (1,2,3,5,7,9,10,11,13,15)$

15 PT.
Problem 15
Repeat problem 14 for a PAL. (You must simplify your answer)

15 PT.
Problem 16
Repeat problem 14 for a PLA. (You must simplify your answer)
Note: you may download blank PLD sheets from
http://www.engr.newpaltz.edu/~bai/EGC220/PLD_symbl.pdf and mark programmable cell with × and fixed cell with ▪.